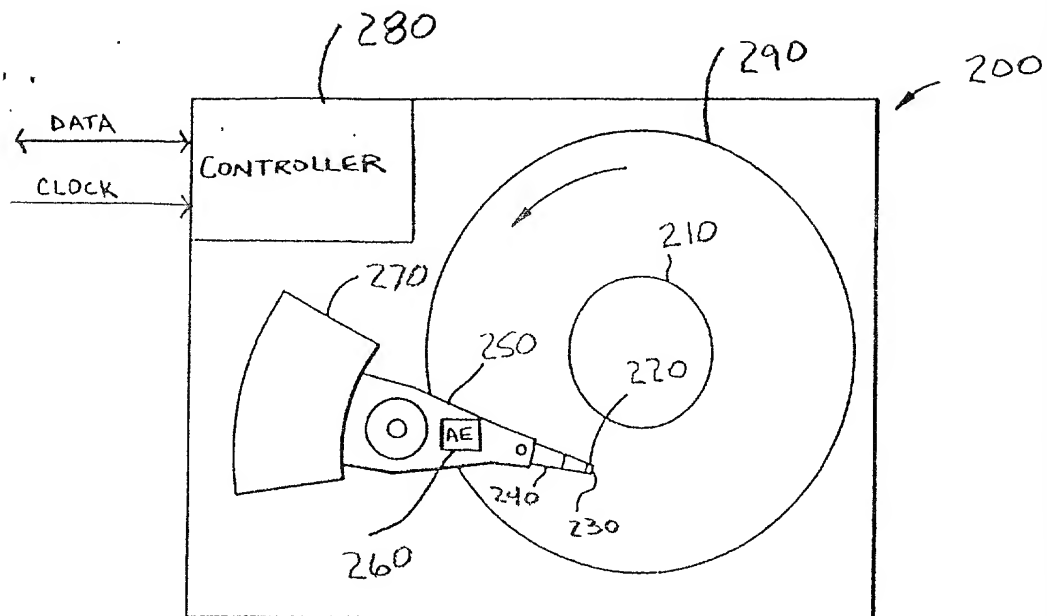


↑
100

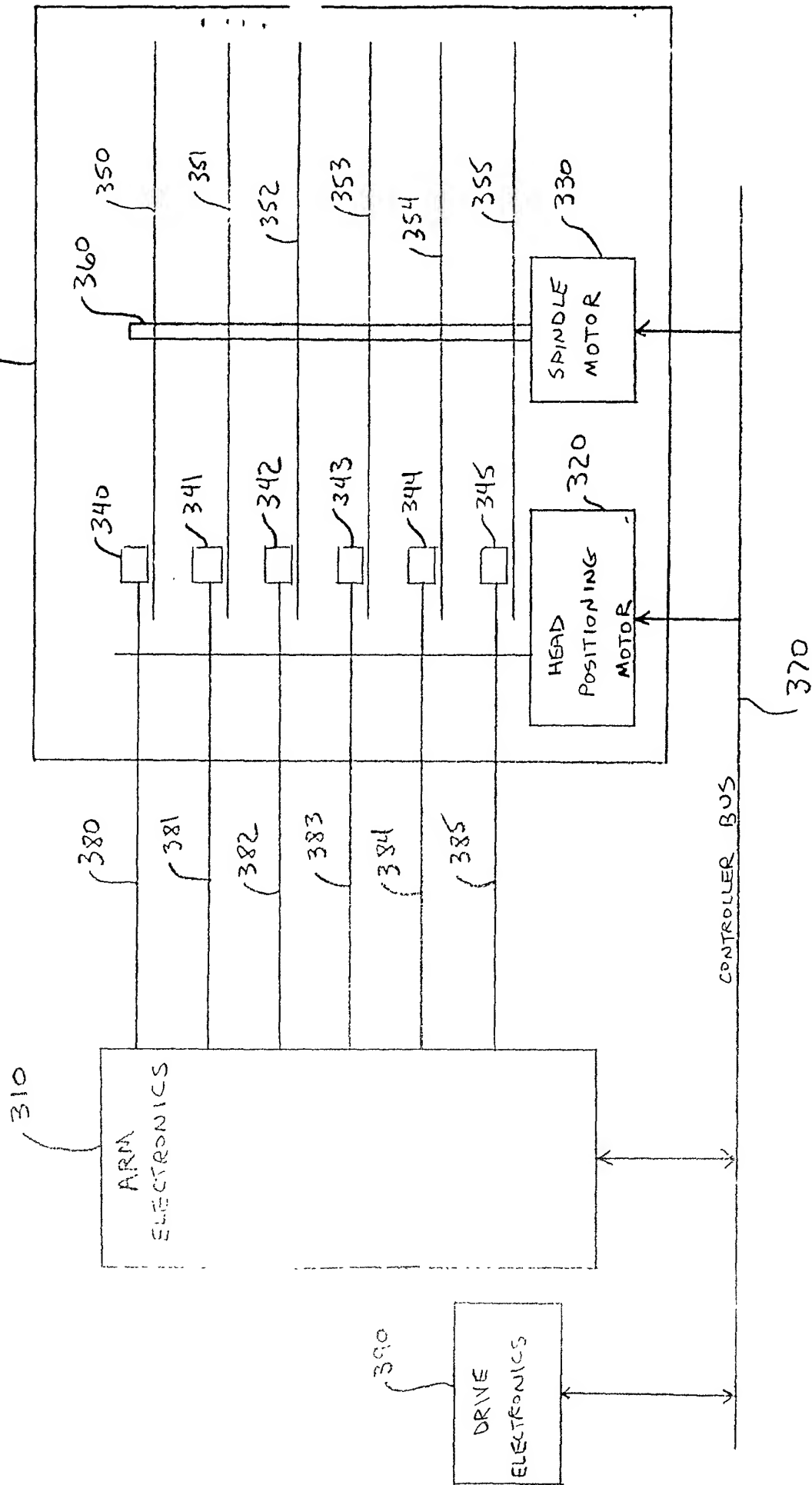
501.407-US-01
VANNORSDEL
FIG. 1



501,407-US-01
 VANNORSDEL
 FIG. 2

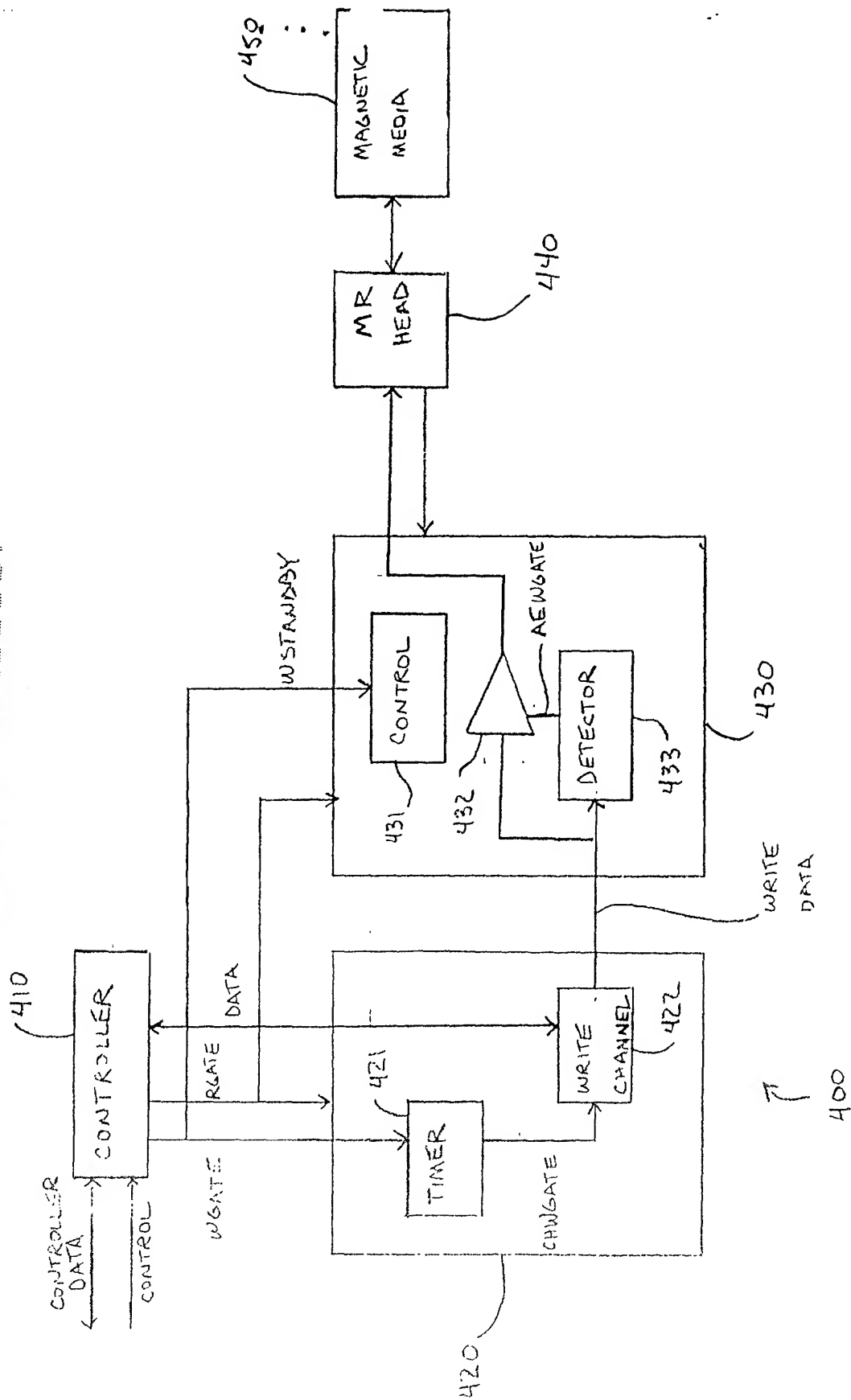
10000448.022402

201.407-01



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VANNOERDEL
FIG. 3

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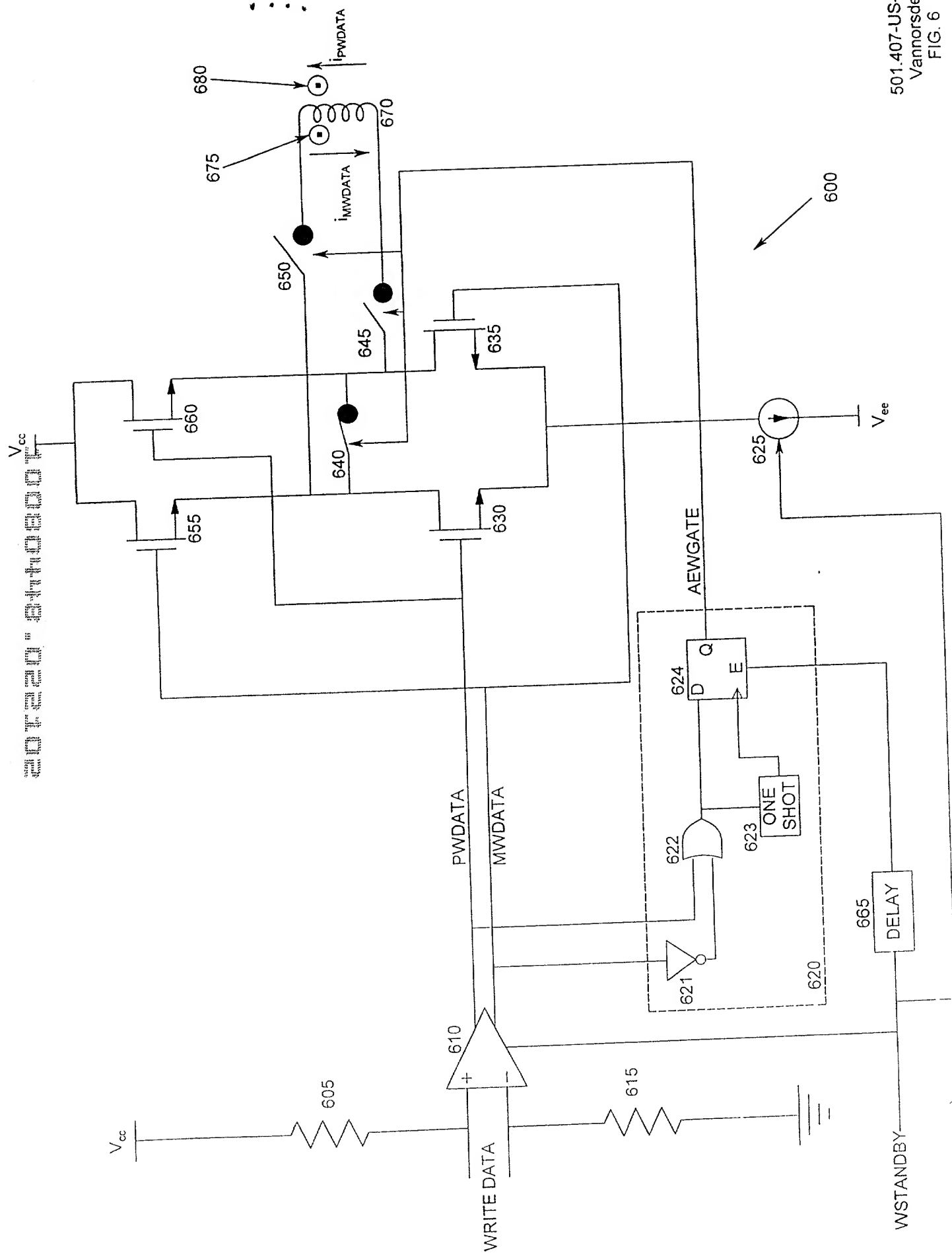
501.407-US-01
VANNORSDEL
FIG. 4

Timing diagram for a memory write operation. The diagram shows five signals over time:

- WGate**: Active low pulse from 500 to 510.
- CnWGate**: Active low pulse from 510 to 520.
- Write Data**: 4-bit data (1011) valid during the CnWGate pulse.
- WStrobe**: Active low pulse from 500 to 510.
- AEWGate**: Active low pulse from 510 to 520.

Time markers are indicated at 500, 510, and 520.

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FIG. 5



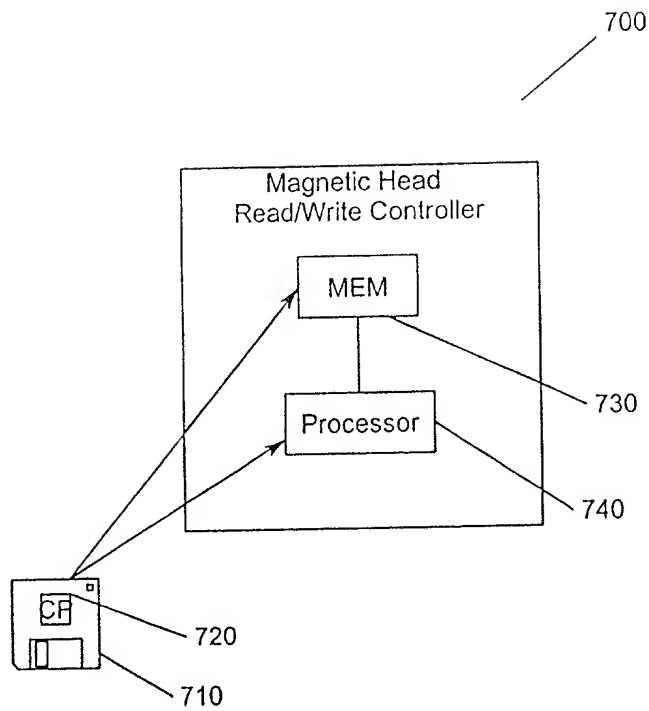
[illegible]

Fig. 7